

at a temperature of 800 to 1100° C wherein said metal segregates in said peripheral portion during the crystallizing; and
etching said peripheral portion after said
crystallizing.

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Upon entry of this amendment, claims 1-3, 5-8, 10-14, and 16-28 will be pending. Claims 26-28 are newly added. All of the remaining claims have been rejected.

The Rejection in View of Nakajima and Gibson

Claims 1-3, 5-8, 10-14, and 16-25 were rejected under 35 U.S.C. § 103(a) in view of Nakajima and Gibson. As stated in Applicant's last response, this application claims priority from Japanese application 7-216608. The filing date of this priority document, August 2, 1995, precedes Nakajima's U.S. filing date of September 8, 1995. Applicant submitted a verified translation of the priority document to the Office on February 26, 1999. Enclosed are copies of the translation and a stamped postcard showing receipt of the translation on March 2, 1999 (Appendix 1).

Therefore, Nakajima does not qualify as prior art under any provision of 35 U.S.C. § 102. Applicant asks the Office to withdraw this rejection.

The Rejections in View of U.S. Patent 5,580,792 ("Zhang")

Claims 1-3, 5-8, 10-14, and 16-25 were rejected under 35 U.S.C. § 103(a) and under the doctrine of obviousness-type double patenting in view of Zhang. Zhang does not show or even suggest "etching the peripheral portions" of a "patterned" semiconductor film, as claimed. The rejection itself acknowledges that Zhang does not etch a patterned film at its peripheral portions (Office action, page 4, lines 4-5), but then attempts to trivialize this distinction by asserting that a person of ordinary skill would have been able "to determine through routine experimentation the optimum, operable placement of [the] etching" described in the Zhang patent (page 4, lines 6-8).

Zhang's etching step is performed on a different portion of the semiconductor film and for a different purpose than the etching step claimed here. Zhang etches the upper surface of the semiconductor film, before patterning, "to expose a clean surface" on which a gate insulating film is later deposited (col. 2, line 65, through col. 3, line 4). Zhang's

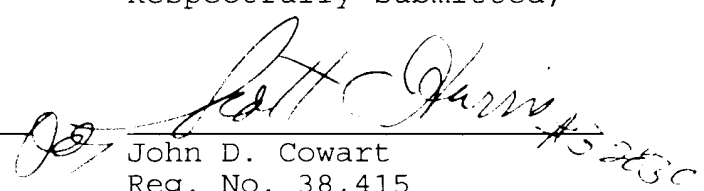
etching does not remove "peripheral portions" of a patterned semiconductor film, as claimed. Zhang does not even suggest that these peripheral portions should be removed. As a result, Zhang's technique yields devices that have higher catalyst concentrations in their active areas than devices produced under the claimed techniques. Therefore, all of the claims are patentable over Zhang.

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

If there are any other charges, or any credits, please apply them to Deposit Account No. 06-1050.

Respectfully submitted,

Date:


John D. Cowart
Reg. No. 38,415

Fish & Richardson P.C.
4225 Executive Square, Suite 1400
La Jolla, California 92037
Telephone: 858/678-5070
Facsimile: 858/678-5099

102953.LJ1